La Cattedrale dell'Elettricità: trasformazione del rudere, permanenza dell’immagine. Il caso della Battersea Power Station di Londra

A pW-Power Hz-Range Oscillator Operating with a 0.3V-1.8V Unregulated Supply

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***Abstract*— In this paper, a pW-power relaxation oscillator for sensor node applications is presented. The proposed oscillator operates over a wide supply voltage range from nominal down to deep sub-threshold, and requires only a sub-pF capacitor for Hz-range output frequency. True pW-power operation is enabled thanks to the adoption of an architecture leveraging transistor operation in super-cutoff, the elimination of voltage regulation and current reference. Indeed, the oscillator can be powered directly from highly variable voltage sources (e.g., harvesters and batteries over their whole charge/discharge cycle). This is achieved thanks to the wide supply voltage range, the low voltage sensitivity of the output frequency and the current drawn from the supply.**

A testchip of the proposed oscillator in 180nm exhibits a nominal frequency of approximately 4Hz, a supply voltage range from 1.8V down to 0.3V with 10%/V supply sensitivity, 8-18pA current absorption, 4%/°C thermal drift from -20°C to 40°C at an area of 1,600µm². To the best of the authors' knowledge, the proposed oscillator is the only one able to operate from sub-threshold to nominal voltage.

***Index Terms*— pW-power, relaxation oscillator, Internet of Things, Ultra Low Power logic style.**

I. Introduction

SLOW oscillators are fundamental building blocks in heavily duty cycled integrated systems that achieve very low power consumption by staying in sleep mode for most of the time, while periodically waking up to perform the intended task [1] (e.g., sensor nodes, Internet of Things devices). Being always on, the power of duty-cycled wake-up oscillators sets the lower bound of the system consumption, and dominates it under low duty cycles [1]-[4]. To retain the benefits of duty cycling in systems with tightly constrained power (e.g., battery-less sensor nodes [3], [5]), significant work has been published to demonstrate wake-up oscillators with deep sub-nW power consumption, recently approaching the pW range [6]-[13]. Such wake-up oscillators need to operate reliably under a wide range of voltages from Volts down to few hundreds of mVs, as summarized in Table I. This table shows the voltage range delivered by different types of harvesters under varying power availability, and batteries throughout their entire discharge cycle [4], [14]-[17]. Existing ultra-low power oscillators generally need to operate in a narrow range (50-100mV) around near- or above-threshold voltages. This makes always-on voltage regulation mandatory, to achieve adequate stability of frequency and power under highly variable power sources, as depicted in Fig. 1. Although not accounted for in the evaluation of most prior oscillators, the quiescent power P_Q drawn by the voltage regulator and other peripheral circuits needed by the oscillator is typically much larger than the oscillator power P_{osc} itself (e.g., references, comparators, bias and control circuitry). This is the case for state-of-the-art linear [18]-[20] and switching regulators [21]-[22] with sub-nW output power, as exemplified in Table II. From this table, the quiescent power of such voltage regulators is generally in the nW range for switching regulators, and in the hundreds of nWs in linear regulators. In [12], [13], the quiescent power for both voltage regulation and reference generation has been respectively

TABLE I. Voltage Range of Energy Sources for Sensor Nodes

type of energy source	V_{MIN}	V_{MAX}
solar cell [4]	140mV	450mV
mixed (solar, thermoelectric) [14]	0.45V	3V
thermoelectric generator [15]	20mV	500mV
Li-Ion cell battery [16]	2.5V	4.2V
Alkaline cell battery [17]	0.8V	1.5V

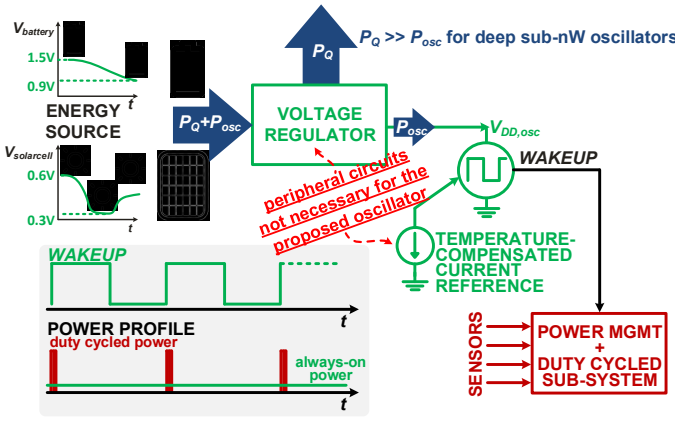

Fig. 1. Wake-up oscillators for duty-cycled sensor nodes, and peripheral circuitry necessary for their operation (e.g., voltage regulator, reference).

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TABLE II. QUIESCENT POWER OF ULTRA-LOW POWER VOLTAGE REGULATORS DELIVERING AN OUTPUT IN THE PW RANGE

	type of regulator	off-chip components	quiescent power
[18]	analog LDO	NO	>350nW
[19]	digital LDO	NO	>4µW
[20]	digital LDO	NO	1.18µW
[21]	switching (boost)	YES	0.5nW
[22]	switching (buck)	YES	760nW

reduced down to 63pW and 49.7pW. Such quiescent power fundamentally limits the system-level benefits coming from the power reduction in the oscillator itself. Hence, ultra-low power oscillators able to operate without voltage regulation and other peripheral circuits would be highly desirable, to preserve their potential power benefit. The ability of oscillators to operate under a wide voltage range (e.g., from sub-threshold to nominal voltage) would also offer additional opportunities to save power and simplify system design. For example, it would allow the oscillator to be directly powered by the harvester in battery-less [3] and battery-indifferent systems [23], avoiding the additional power contribution due to conventional voltage up-conversion occurring between the harvester and the above mentioned voltage regulator.

Overall, the proposed oscillator has a power consumption that is anyway lower than prior art by a factor of 13-1,750X compared to [6]-[9], [11]-[13], even without considering the actual power cost of voltage regulation and reference generation in [6]-[9] and [11]. The only oscillator in the pW range [10] does not account for the above additional power cost. Even extrapolating the power cost of voltage regulation and reference generation from [12], [13] and attributing it to [10] (which has not been demonstrated on silicon), such power cost is in the range of tens of pWs (28% of 224pW in [13], 49.7pW in [12]). This is an order of magnitude larger than the targeted pW range (e.g., 3.3pW in the proposed oscillator), and hence dominates over the oscillator consumption anyway.

On a broader perspective and beyond the above considerations on the voltage sensitivity, the proposed oscillator has the unique property that it truly operates from nominal voltage down to deep sub-threshold (e.g., 0.3V). This adds further flexibility and opportunities to save power and simplify system design, for example in energy harvested and battery-less systems. For example, harvesters (e.g., solar cell, rectified AC vibration-based harvester) with output voltage above 300mV can directly power the oscillator, eliminating the need for traditional harvester voltage up-conversion, whose power would otherwise add to the power cost of the successive LDO. As another example, the ability of the proposed oscillator to operate across a wide voltage range allows operation under large variations in the harvester voltage under a given voltage conversion ratio, and hence at lower levels of harvested power since significant supply voltage reduction is tolerated by the oscillator (e.g., lower light intensity for a solar cell-powered system).

In this paper, a relaxation oscillator able to operate from nominal voltage down to deep sub-threshold, at pW-level power consumption and Hz-range frequency is presented [2]. The low sensitivity of the oscillation frequency and the supply current allows the elimination of the voltage regulator and its related power contribution, thus enabling direct powering from the harvester or the battery. Further power reduction is enabled by the suppression of the temperature-compensated current reference, as allowed by the many applications where the temperature is naturally restricted to a limited range [8] (e.g., wearable electronics, implantable circuits, indoor sensing, smart clothing, food supply chain management). Accordingly, temperature compensation was dropped in the proposed oscillator, reaching a net power consumption of 3.3pW at room temperature and 0.4V supply.

This paper is structured as follows. The proposed oscillator architecture and its main building blocks are described in Section II. Circuit-level operation of the proposed oscillator and sensitivity to the supply are analyzed in Section III. The testchip design and the measurement results are reported in Section IV, where comparison with the state of the art is presented. Conclusions are drawn in Section V.

II. PROPOSED DIGITAL OSCILLATOR ARCHITECTURE AND DESCRIPTION OF BUILDING BLOCKS

The proposed relaxation oscillator is based on the digital architecture in Fig. 2, where the logic gates determine the oscillation through the periodic (dis)charge of the on-chip flying capacitor C. All logic gates are implemented in the Dynamic Leakage Suppression (DLS) logic style [3], originally introduced in [5] and also known as Ultra-Low Power (ULP) logic. As will be detailed in the following section, the adoption of the DLS logic style is essential for the intended operation of the architecture in Fig. 2 for various reasons. First, DLS logic gates deliver very small and nearly supply-independent ON current I_{DLS} (~3pA/gate in 180nm), thus allowing the intended slow oscillation at compact capacitor C. Second, the dominant static power of DLS logic is determined by a current lower than the regular transistor leakage at zero gate-source voltage, thus leading to very low power consumption. Third, DLS logic gates exhibit hysteretic behavior, which is exploited to create proper and nearly supply-independent hysteresis thresholds for the voltage across C, which in turn define the oscillation period.

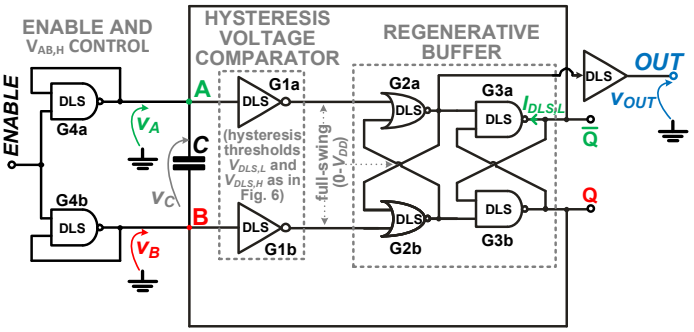

Fig. 2. Gate-level architecture of the proposed wake-up oscillator.

The architecture in Fig. 2 comprises three main building blocks around the flying capacitor C. The inverters G1a-b sense voltages v_A and v_B, acting as voltage comparators with hysteresis (see detailed operation in Subsection A). The outputs of G1a-b drive the NOR-based SR latch G2a-b, which periodically regenerates and holds the output at the high or low level. The output of G2a is buffered to generate the oscillator output, and drive the external load. The NAND-based SR latch G3a-b provides the necessary inversion to establish a positive feedback loop and sustain the oscillation, as usual in relaxation oscillators. G3a-b are in turn loaded by G4a-b, which act like inverters with short-circuited input/output once $ENABLE$ is asserted, i.e. they serve as an active load. In turn, the presence of the active load G4a-b sets the high logic output voltage of gates G3a-b, which is named $V_{AB,H}$ in the following.

When necessary, the oscillation can be inhibited by de-asserting the $ENABLE$ signal in Fig. 2. Indeed, when $ENABLE$ is set at the ground voltage, nodes A and B are both set high by the NAND gates G4a-b independently of the state of Q and $\bar{Q}$, thus breaking the positive feedback loop. Accordingly, G4a-b also serve the additional purpose to gate the entire oscillator.

As will be detailed in Section III, under a given capacitor C and ON current, the oscillation period is defined by the voltage swing at v_A and v_B. Such voltage swing will be shown to be lower bounded by the low hysteresis threshold $V_{DLS,L}$ of the comparator G1a-b, and the maximum voltage V_{MAX} achievable by nodes A and B. The former is dictated by the DLS comparator G1a-b, whereas the latter is set by the latch G3a-b with the active load G4a-b. The circuit parameters that determine these voltages in DLS gates and in the latch with active load are respectively analyzed in Subsection A and B below. Interesting properties that were not noticed in the original papers [3], [5] will be highlighted in the following. The resulting properties will be then used to analyze the overall operation of the oscillator in Section III.

A. Dynamic Leakage Suppression (DLS) Logic and Hysteresis

The DLS (or also ULP) logic style was proposed and demonstrated in [3], [5] to reduce the OFF power well below the regular transistor leakage (i.e., at zero gate-source voltage), although at the cost of drastically reduced speed. The schematic of a DLS inverter gate is depicted in Fig. 3, where the pull-up (pull-down) network consists of transistor MPU (MPD) as in a standard CMOS inverter gate. In general, the DLS pull-up and pull-down networks in any cell are the same as standard CMOS cells. As a major difference, DLS logic gates include an NMOS header transistor MN and a PMOS footer MP, whose gate terminal is driven by the cell output, thus creating a feedback loop.

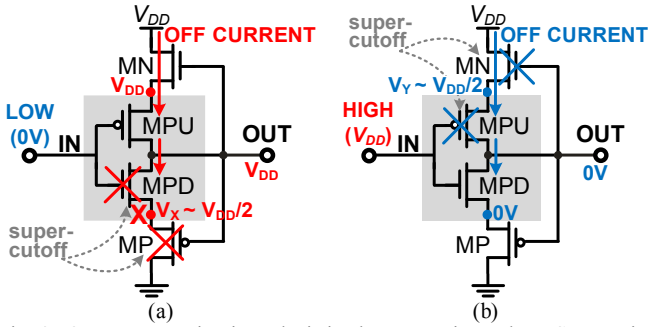

Fig. 3. OFF current circuit analysis in the Dynamic Leakage Suppression (DLS) inverter gate at a) high and b) low output.

In regard to the OFF current drawn by DLS logic gates, Fig. 3a shows that a low input turns off MPD and determines a high output, which in turn switches off the PMOS footer MP. Since the drain currents of MPD and MP are the same, the voltage V_x of their common node settles to a value that is close to $V_{DD}/2$ [3], [5]. This translates into a negative gate-source (source-gate) voltage in MPD (MP) around $-V_{DD}/2$, and hence operation in super-cutoff. Dual considerations hold for a high input, which determines super-cutoff operation in MN and MPU as shown in Fig. 3b. This explains why the OFF current of DLS logic gates is 2-3 orders of magnitude below the regular leakage current and in the order of 10fA/gate in 180nm CMOS [3].

The ON current I_{DLS} of DLS cells is equal to the intrinsic leakage of the NMOS header (PMOS footer) during an output rising (falling) transition, i.e. the transistor current at zero gate-source voltage [3]. Interestingly, this ON current is very small and nearly supply-independent at first order[1]. The small ON current allows slow operation as desired in wake-up oscillators, thus requiring relatively small additional flying capacitors to achieve low oscillation frequencies. For example, DLS gate delays are in the millisecond range in 180nm CMOS, and a sub-pF load capacitance is sufficient to achieve oscillation gate delays in the sub-second range, and hence an oscillation frequency in the Hz range. Also, the nearly supply-independent ON current allows relatively stable oscillation frequency in spite of wide V_{DD} fluctuations, as required by operation with unregulated supply (see detailed analysis in the next section).

The proposed oscillator architecture also leverages the hysteretic behavior of DLS gates, which is determined by the positive feedback loop enabled by the connection of the cell output to the gate terminal of MP and MN in Figs. 3a-b [3], [5]. Fig. 4a shows that the high-to-low threshold $V_{DLS,H}$ in 180nm CMOS at V_{DD}=400mV is 250mV and expectedly larger than $V_{DD}/2$=200mV. The low-to-high threshold $V_{DLS,L}$ is 70mV, and hence lower than $V_{DD}/2$. As an interesting observation, both DLS hysteresis thresholds weakly depend on V_{DD}, as can be seen from the plot of the hysteresis thresholds versus V_{DD} in Fig. 4b. This is very different from standard CMOS logic gates, whose logic threshold is in the neighborhoods of $V_{DD}/2$ [24], and therefore tracks the supply voltage. From Fig. 4b, the low hysteresis threshold $V_{DLS,L}$ exhibits a minor supply sensitivity of less than 10mV/V in the 0.3-1.8V supply range. From (A.5) in Appendix A, $V_{DLS,L}$ is mainly determined by the thermal voltage $V_T = kT/q$, where k is the Boltzmann constant, T is the absolute temperature, and q is the electron charge. Hence, $V_{DLS,L}$ does not depend on V_{DD} to a first order.

[1] More precisely, the current delivered by MN (MP) in a falling (rising) output transition slightly depend on V_{DD} through the DIBL effect.

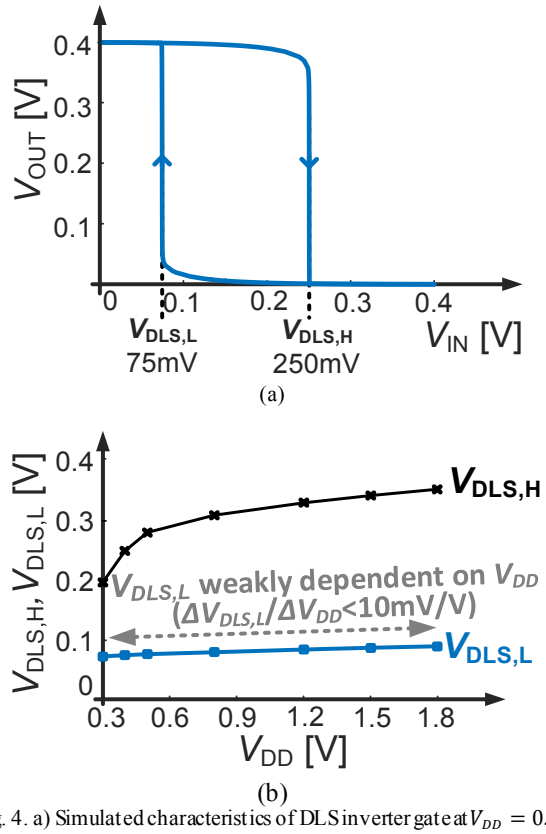

Fig. 4. a) Simulated characteristics of DLS inverter gate at $V_{DD} = 0.4$V showing hysteresis thresholds, b) plot of hysteresis thresholds vs. V_{DD}.

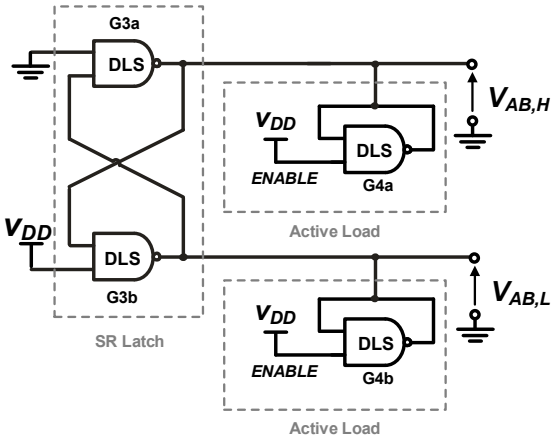

Fig. 5. Equivalent gate-level description of the circuit from Fig. 2 for the evaluation of the output voltage of the DLS latch G3a-b loaded by G4a-b.

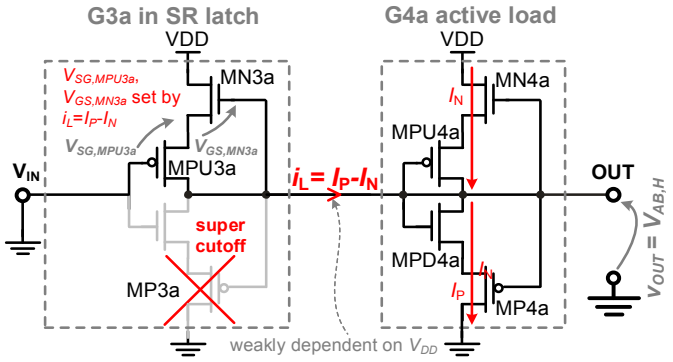

Fig. 6. Transistor-level equivalent circuit of Fig. 5 for the evaluation of $V_{AB,H}$.

B. Analysis of DLS Latch with Active Load

In this section, the DC output voltage of the latch G3a-b loaded by G4a-b is discussed, as necessary for the evaluation of the oscillation frequency in the next section. The latch output voltage will be shown to be nearly supply-independent thanks to the presence of the active load G4a-b in Fig. 2, as opposed to an unloaded DLS cell whose output is at either ground or V_{DD}.

When *ENABLE* is asserted in Fig. 2, logic gates G4a-b act like inverters with short-circuited input/output as shown in Fig. 5, which clamp the outputs of G3a-b to non-full swing voltages (i.e., lower than V_{DD}, and higher than ground). Assuming that one of the inputs of G3a is low and the other is high, $V_{AB,H}$ is set by G3a and G4a in Fig. 5, which can be represented as equivalent DLS inverter gates as in Fig. 6 (i.e., the NAND pull-up and pull-down networks are replaced by a single equivalent transistor).

As detailed in Appendix B, circuit analysis of Fig. 6 shows that $V_{AB,H}$ is set by the gate-source voltages across transistors MN3a and MPU3a, which in turn depend on the current difference $I_P - I_N$ of the pull-down and pull-up networks of the active load. In turn, the currents I_N and I_P are equivalent to the ON current delivered by a DLS inverter gate, which is nearly supply-independent [3], as discussed in the previous subsection and in Appendix B. The supply voltage independence of $V_{AB,H}$ is confirmed by the simulation results in Fig. 7, where transistors are minimum sized. In particular, $V_{AB,H}$ is about 275mV, and shows a weak sensitivity to the power supply of 60mV/V for V_{DD} widely ranging from 0.3V to the nominal voltage 1.8V. By similar considerations, the low latch output $V_{AB,L}$ under the active load G4a-b is about 32mV and nearly independent of V_{DD}. In the next section, the above properties will be shown to be essential for the supply voltage independence of the oscillator frequency.

III. Circuit Analysis of the Proposed Oscillator and Supply Sensitivity

In this section, the operation of the proposed oscillator is described in Subsection A, based on the properties of building

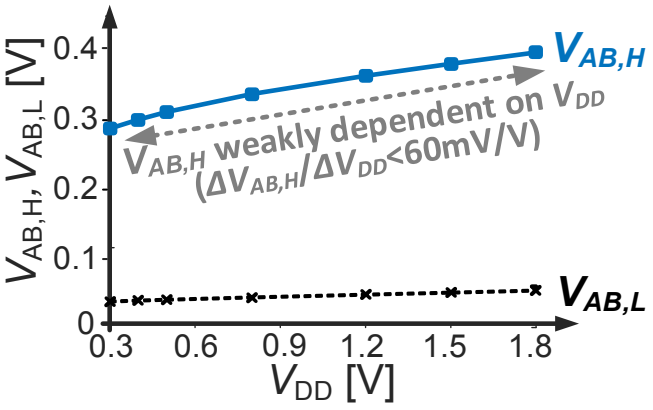

Fig. 7. Output voltage levels $V_{AB,H}$ and $V_{AB,L}$ of the latch G3a-b loaded by G4a-b in Fig. 2.

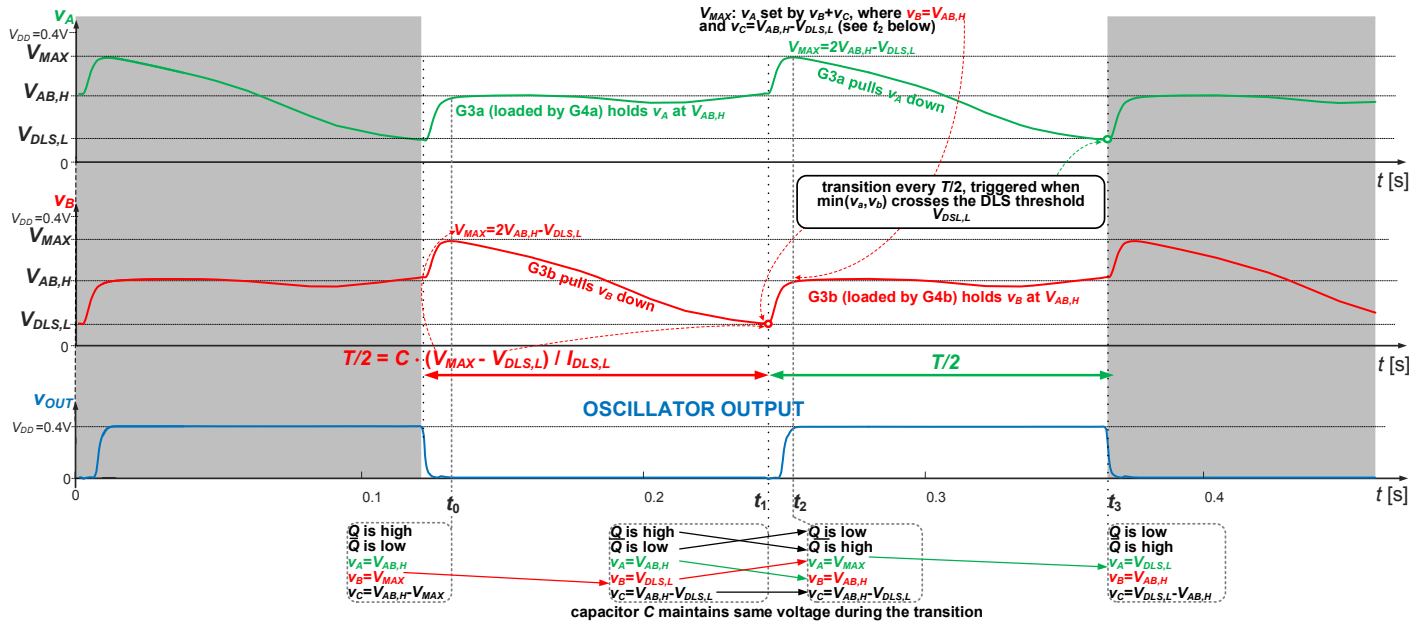

Fig. 8. Operation of the proposed oscillator and related waveforms showing how the oscillation period is formed.

blocks in the previous section. The supply independence of the oscillation frequency is then discussed in Subsection B.

A. Relaxation Oscillator Operation

When $ENABLE$ is de-asserted in Fig. 2, the circuit is reset since the nodes A, B, Q and $\bar{Q}$ signals (via G2a-b and G3a-b gates) are constantly set at the low logic level. When $ENABLE$ is asserted, latches G2a-b and G3a-b are driven to the hold state, and hence set $\bar{Q}$ high (Q low) or low (high) depending on the relative delay through the paths going from A to $\bar{Q}$ (B to Q), as dictated by random variations. In either case, the oscillation is initiated as depicted in Fig. 8, starting either from the first or the second half-period. In particular, let us assume that the output $\bar{Q}$ (Q) in Fig. 2 is high (low) at the reference time t_0, as depicted in Fig. 8. At $t = t_0$, v_A is accordingly set to the supply-independent voltage $V_{AB,H}$ by logic gates G3a-b, thanks to the effect of the active load G4a-b discussed in Section IIIB. $V_{AB,H}$ in Fig. 8 is about 200mV from the considerations at the end of Appendix B. At the same time, v_B is set to $V_{MAX} > V_{AB,H}$ from the end of the previous period, as it will be discussed later on. Being both v_A and v_B higher than the low hysteresis threshold $V_{DLS,L}$ of G1a-b, the outputs of G1a-b are therefore both low and force the latch G2a-b in the hold state. Since the output $\bar{Q}$ (Q) of G3a-b is opposite to the input of G3a (G3b) due to the inverting behavior of the NAND-based latch, the output of G2a is low and hence drives the oscillator output at the low level.

After $t = t_0$, v_B is pulled down by the output of G3b, which draws a nearly supply-independent current I_{DLS}, as discussed in Section II. Such constant current slowly discharges C with a nearly-constant slope $dv_B/dt = -I_{DLS}/C$, until v_B crosses the low hysteresis threshold $V_{DLS,L}$ of G1b at $t = t_1$. At this point of time, the voltage across the capacitor C is $v_C = v_A - v_B = V_{AB,H} - V_{DLS,L}$. Right after $t = t_1$, the input of G1b determines its output rising transition, which in turn triggers a falling transition at the output of G2b, and a rising transition at the output of G3b, thus raising v_B to $V_{AB,H}$ at $t = t_2$. Since capacitor C maintains the same voltage during the transitions, v_A is raised at $V_{MAX} = V_{AB,H} + v_C = V_{AB,H} + (V_{AB,H} - V_{DLS,L}) > V_{AB,H}$, which is 330mV from Fig. 8. This makes the current delivered by the active load G4a nearly zero, as it induces operation in super-cutoff in its pull-up network like any other DLS gate, as discussed in Section II. Interestingly, V_{MAX} is above the DC high output level $V_{AB,H}$ of G3a-b, in a fashion that is similar to the behavior of self-oscillating charge pumps [27]. Correspondingly, $\bar{Q}$ starts being pulled low by G3a, due to the inverting nature of G1a, the NOR-based latch G2a-b and the NAND-based latch G3a-b. Overall, the above sequence from t_0 to t_2 defines the first half oscillation period.

After $t = t_2$, $\bar{Q}$ is low, Q is high, and the oscillator output is high, as opposed to the initial circuit state. The same qualitative behavior described above is expectedly observed due to the circuit symmetry in Fig. 2, by simply swapping Q and $\bar{Q}$, v_A and v_B. At the end of the second half period at $t = t_3$ in Fig. 8, v_A drops to the extent that it crosses again the low hysteresis threshold $V_{DLS,L}$ of the comparator G1a-b. Subsequently, node B is pulled up to V_{MAX} as discussed above, thus reinstating the initial conditions that were assumed at the beginning of the section. Such second half period is again defined by the discharge of capacitor C from V_{MAX} down to $V_{DLS,L}$, through the current I_{DLS} delivered by the latch G3a-b. In other words, the second half period has the same duration as the first half, and depends on the low hysteresis threshold $V_{DLS,L}$ of G1a-b, while it is independent of $V_{DLS,H}$. Then, periodic oscillation is observed once the initial conditions at t_0 are restored.

Interestingly, although the circuit symmetry would suggest fully differential operation, the waveforms in Fig. 8 clearly show that this is not the case. In other words, the signal pair Q and $\bar{Q}$ (and any other pair of symmetric signals) is not

associated with voltages that are opposite with respect to some common-mode voltage.

The next subsection focuses on the supply voltage independence of the oscillation frequency, leveraging the supply independence of $V_{DLS,L}$ and $V_{AB,H}$.

B. Analytical Expression of the Oscillator Frequency and Power Supply Sensitivity

Based on the above analysis, the relaxation oscillator has a duty cycle of 50%. The half period is equal to the fall time $t_1 - t_0$ of v_B (or v_A) from V_{MAX} to $V_{DLS,L}$, plus the internal transition time $t_2 - t_1$. Since $v_A = V_{AB,H}$ is nearly constant during the falling transition of v_B from Fig. 8, the slope of the voltage drop in v_B is equal to the slope of the voltage v_C. The latter is due to the discharge of C at constant current I_{DLS}, so that the slope of v_C is I_{DLS}/C. Neglecting the small transition time $t_2 - t_1$ (less than 4% of the period), the oscillation period is expressed as

$$T \approx 2\frac{C}{I_{DLS}}\left(V_{MAX} - V_{DLS,L}\right) = 4\frac{C}{I_{DLS}}\left(V_{AB,H} - V_{DLS,L}\right). \quad (1)$$

From (1), the oscillator supply independence is enabled by the weak supply dependence of the voltage swing $\left(V_{AB,H} - V_{DLS,L}\right)$ across the capacitor setting the period, and of the current delivered by DLS gates. The supply independence of the former is enabled by the interesting observation that the low DLS hysteresis threshold is nearly independent of V_{DD}, like the high output voltage of DLS gates loaded by the active load G4a-b.

In regard to the temperature dependence of (1), the main contribution is due to the I_{DLS} current, being the simulated thermal drift of $V_{AB,H} - V_{DLS,L}$ 142X lower than the former. Regarding the supply dependence of the current drawn by the oscillator, the latter is dominated by the sub-threshold leakage current, which is again relatively insensitive to V_{DD} [3], [5] (the weak dependence on V_{DD} is determined by the DIBL effect). More specifically, the supply sensitivity of I_{DLS} was found to be 30%/V, whereas the sensitivity of $V_{AB,H} - V_{DLS,L}$ is 22%/V. Since both I_{DLS} and $V_{AB,H} - V_{DLS,L}$ increase with the supply, their individual supply sensitivity is in part compensated in the period expression (1), which depends on their ratio. This is very different from other relaxation oscillators based on standard CMOS logic or analog circuitry, whose consumption typically has a strong dependence on the supply voltage. Indeed, standard CMOS logic gates draw a power that changes by several orders of magnitude when V_{DD} is increased from low voltages (e.g., near- or sub-threshold) to nominal voltage. Similarly, analog circuits (e.g., amplifiers, comparators) require the key transistors operate in a narrow range around their nominal bias point, which in turn tightly constraints the range of allowed voltages [6]-[13].

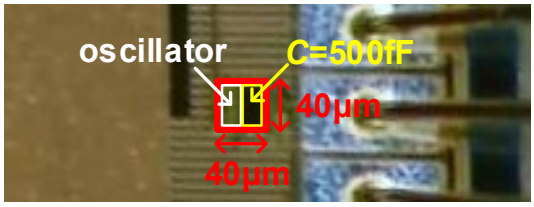

Fig. 9. Micrograph of the testchip implementing the proposed oscillator.

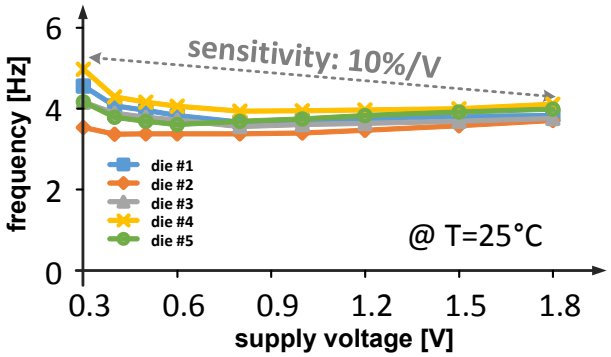

Fig. 10. Measured oscillation frequency vs V_{DD} at room temperature (T=25°C) across five dice.

The proposed oscillator exhibits the unprecedented ability to operate without voltage regulation, being capable to maintain nearly the same oscillation period and consumption across a wide supply range, from sub-threshold to nominal voltage.

IV. Testchip Design and Measurement Results

The proposed relaxation oscillator was demonstrated through a 180nm testchip, whose micrograph is shown in Fig. 9. The testchip was designed with an automated digital design flow, after creating a standard cell library of DLS gates with minimum size. A Metal-Oxide-Metal (MOM) on-chip capacitor C of 500fF was also instantiated.

The circuit occupies a silicon area of 1,600 µm^2, which is the second smallest among [6]-[13]. Fig. 10 shows the frequency measured over five dice at nominal temperature (25°C) and supply of 0.4V, when averaged over three hours (i.e., 43,200 periods). The resulting oscillation frequency ranges from 3.36Hz to 4.28Hz, and has an average of 3.87Hz. From Table III, the sensitivity to process variations is the lowest reported, with a variability of 8.9%, which is slightly better than [11], and 1.9-3.1X better than [6], [12].

As expected from the considerations in Section III.B, the oscillation frequency is relatively independent of V_{DD}, as quantified by the 10%/V voltage sensitivity. This translates into a frequency change of percentage points when V_{DD} typically fluctuates by a few hundreds of mVs, and 10% change when V_{DD} widely fluctuates from sub-threshold to nominal voltage.

The measured current drawn from the 0.4-V supply ranges from 7.3pA to 9.5pA over five dice, corresponding to a power consumption ranging from 2.9pW to 3.7pW, with an average of 3.32pW. The current drawn by the proposed oscillator shows a weak dependence on V_{DD}, as it remains below 20pA over the entire 0.3-1.8V voltage range, as shown in Fig. 11. The resulting supply sensitivity of the current drawn by the oscillator is 8pA/V.

The same dice were also characterized versus temperature at the same 0.4V supply, as shown in Fig. 12. Not being temperature-compensated, the frequency shows a mean thermal drift of 4%/°C from -20°C to 40°C. This is comparable to the uncompensated oscillator in [10], and expectedly higher than temperature-compensated oscillators [8]-[9], [12]-[13]. Like prior uncompensated oscillators [10]-[11], the thermal drift is

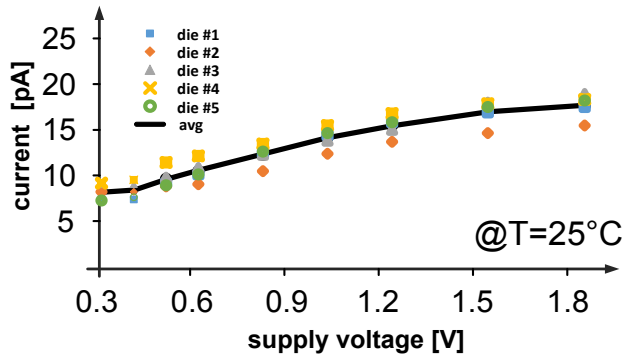

Fig. 11. Measured current drawn from the supply vs V_{DD} at room temperature (T=25°C) across five dice.

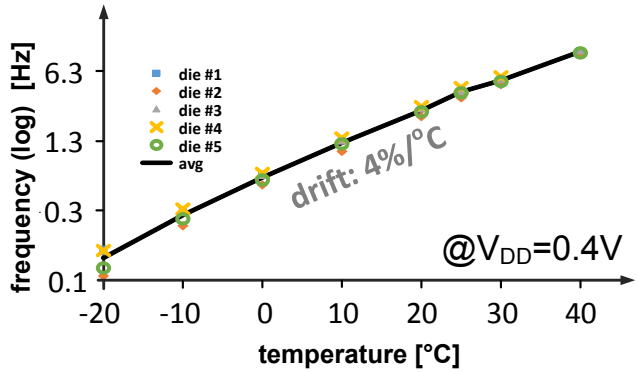

Fig. 12. Measured oscillation frequency vs temperature at V_{DD}=0.4V across five dice.

acceptable for the targeted applications with naturally limited temperature fluctuations (see Introduction).

The long-term stability of the proposed oscillator was tested by measuring the Allan deviation of the frequency versus the observation time, as plotted in Fig. 13. From this figure, the Allan deviation reaches a minimum of about 10^{-3} at approximately one-hour observation time. This time period is relevant to the targeted range of applications, and is the same order of magnitude of other ultra-low power relaxation oscillators [11]-[13]. The histogram of the oscillation frequency over 3-hour time (i.e., 43,200 periods) is also reported in Fig. 14. The resulting standard deviation of the frequency drift is 14mHz, which amounts to 0.39% of the time-averaged period.

Table III compares the proposed oscillator with recent prior art in low-frequency wake-up relaxation oscillators for heavily-duty cycled sensor nodes. From this table, the proposed

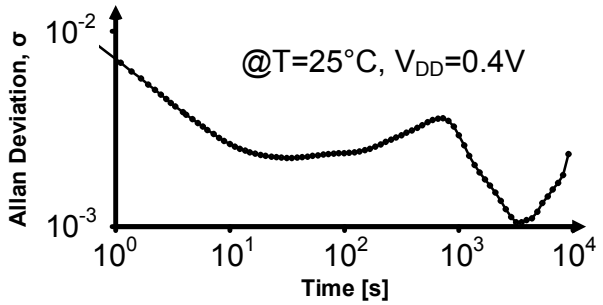

Fig. 13. Measured Allan deviation of the oscillation frequency over 3-hour time window at room temperature (T=25°C) and V_{DD}=0.4V.

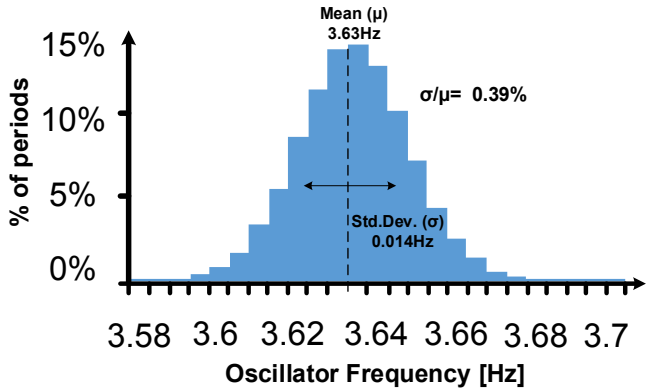

Fig. 14. Histogram of the oscillation frequency over 3 hours at nominal temperature (T=25°C) and supply voltage V_{DD}=0.4V.

oscillator exhibits the lowest operating voltage of 0.3V, and the widest supply voltage range from 0.3V to 1.8V, which is 15-37.5X wider compared with [6]- [8], [11], [12]. The voltage range of the proposed oscillator includes sub-threshold and near-threshold operation, as opposed to other oscillators, including [13] that adopts I/O devices to widen the voltage range. Compared to [9], the proposed oscillator reduces the minimum operating voltage from 1.2V down to 0.3V. In spite of the absence of voltage regulation, the supply sensitivity of the oscillation frequency is still significantly smaller (i.e., by 5X or more) than voltage-regulated oscillators in [6], [7], [8], [10], [11].The supply sensitivity of the oscillation frequency is the second lowest after [9] . The ability to retain nearly the same frequency and low power consumption across a wide range of V_{DD} enables operation under an unregulated supply. To the best of the authors' knowledge, the proposed oscillator is the only one that is able to operate from sub-threshold to nominal voltage.

The oscillator in this work shows the lowest power consumption of 3.3pW at 0.4V supply, which is about 25% lower than the best competitor [10], and 13-1,700X lower than others [6]-[9], [11]-[13]. The actual power advantage over [6]-[11] is substantially larger, when the quiescent power of the on-chip voltage regulator is fairly taken into account (see Table II).

V. Conclusion

A pW-power, Hz-range, digital relaxation wake-up oscillator has been presented in this paper. The oscillator is based on a non-fully differential architecture and leverages a few interesting observations on the adopted DLS logic style [3], [5]. First, the current delivered to the load by such logic gates is very small (pA range), thus allowing Hz-range operation with small on-chip capacitors, Second, this current is rather insensitive to the supply, along with the low hysteresis threshold of such logic gates. Third, the high output voltage of DLS gates with active load is also supply voltage-independent. Fourth, the static current drawn by the adopted logic style, and hence the oscillator power, is also voltage-independent. The supply voltage independence of supply current and frequency allow the suppression of the voltage regulator, whose power typically overwhelms the consumption of the oscillator.

TABLE III. COMPARISON TABLE OF STATE-OF-THE-ART WAKE-UP RELAXATION OSCILLATORS (BEST PERFORMANCE IN BOLD)

	[6] Lin CICC07	[7] Lin ISSCC09	[8] Lee JSSC13	[9] Jeong JSSC15	[10] Nadeau JSSC16	[11] Wang JSSC16	[12] Wang ESSCIRC17	[13] Lim VLSI18	This work
Technology [nm]	130	130	130	180	180	65	65	55	180
Oscillator principle	gate leakage	program & hold	gate leakage	RC	program & hold	capacitor discharge	relaxation	ring oscillator	digital with DLS
Supply voltage [V]	0.45	0.6	0.7	1.2	0.6	0.5	0.6	1.2	0.4
Power [pW]	120	150	660	5,800	4.2	44.4	124.2**	224**	**3.32**
Energy efficiency [pJ/Cycle]	1,333	13.5	1,784	527.2	0.23	15.86	13.3	2.49	0.83
Frequency [Hz]	0.09	11.11	0.37	11	18	2.8	9.3	90	4
Frequency spread (σ/μ)	28%	N/A	N/A	N/A	N/A	11.8%	17.2%	N/A	8.9%
Voltage range [V]	0.4 to 0.5	0.55 to 0.65	0.65 to 0.75	1.2 to 2.2	N/A	0.48 to 0.52	0.6 to 1.1	1.1 to 3.3	**0.3 to 1.8**
Supply sensitivity [%/V]	150	60	420	1	50	160	1.6	0.93	10
Temperature range [°C]	0 to 80	0 to 90	-20 to 60	-10 to 90	-30 to 60	-40 to 60	-40 to 120	-5 to 95	-20 to 40
Thermal drift [ppm/°C]	1,600	490	31	45	20,000	1,260	999.9	260	42,000
Frequency shift for 10% supply voltage, 5°C temperature change	7.55%	3.85%	29.42%	**0.14%**	24.40%	8.63%	0.6%	0.24%	21%
Area (μm^2)	**480**	19,000	15,300	240,000	N/A	25,500	9,100	57,000	1,600
Area* ($10^3 \cdot F^2$)	**28.4**	1124.3	905.3	7407.4	N/A	6,035.5	2,153	18,840	49.4
Offline calibration	N/A	N/A	multi-point calibr.	N/A	N/A	no calibration	no calibration	3-point calibr.	no calibration
Additional voltage regulator / current reference required	YES / NO	YES / NO	YES / YES	YES / YES	YES / YES	YES / NO	YES/YES	YES/YES	**NO / NO**
Allan deviation floor [ppm]	N/A	N/A	N/A	**< 60**	N/A	< 550	<220	<500	< 1,000

* F = minimum feature size of the process
** measured power consumption includes the regulator and reference power

A 180nm testchip of the proposed oscillators occupies 1,600μm², and operates at the lowest reported power supply voltage of 0.3V, and over the widest power supply voltage range from 0.3V to 1.8V. Quantitatively, the supply sensitivity of the output frequency is 10%/V, and the sensitivity of the current absorption is 8pA/V. The thermal drift of the frequency shows a mean thermal drift of 4%/°C, which is comparable with other oscillations without thermal compensation.

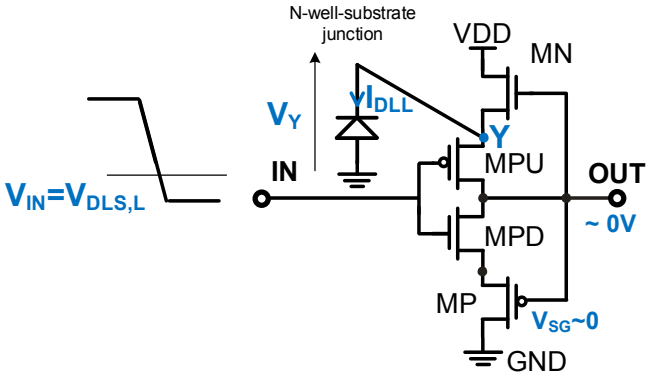

Fig. 15. Schematic of a DLS inverter correspondence of the high-to-low input transition considered in the evaluation of the low switching threshold

The power consumption is 1.25-1,700X lower than the recent state of the art [11]-[13], and such power advantage further increases when fairly accounting the typical consumption associated with voltage regulation [6]-[11]. Thanks to these properties, the proposed oscillator is well suited for direct powering from low-voltage and/or highly-variable energy sources such as energy harvesters and batteries across their entire discharge cycle. To the best of the authors' knowledge, the proposed oscillator is the only one that is able to operate from sub-threshold to nominal voltage.

APPENDIX A. EVALUATION OF $V_{DLS,L}$

The lower hysteresis threshold voltage $V_{DLS,L}$ for a DLS inverter can be estimated with the aid of the circuit in Fig. 15 where all transistors operate in the sub-threshold region, and their NMOS drain current is hence expressed as [25]

$$i_D = I_0 e^{\frac{v_{GS}}{nV_T}}\left(1 - e^{-\frac{v_{DS}}{nV_T}}\right) \quad \text{(A.1)}$$

where the sub-threshold slope factor n and the current I_0 are assumed equal for all the devices, and $V_T = kT/q$ is the thermal voltage. As usual, the PMOS current is obtained by replacing v_{GS} by v_{SG}, and v_{DS} by v_{SD}. Assuming that the input voltage V_{IN} is initially high, KCL at node Y yields

$$e^{\frac{V_{SG,MPU}}{nV_T}} + \frac{I_{DLL}}{I_0} = e^{\frac{V_{GS,MN}}{nV_T}} \quad \text{(A.2)}$$

where the leakage current I_{DLL} in Fig. 15 is associated with the reverse-biased n-well to substrate pn junction in MPU.

Expressing $V_{SG,MPU}$, $V_{SG,MN}$ in terms of V_y and V_{in}, (A.2) leads to

$$e^{\frac{V_y-V_{in}}{nV_T}}\left(1+\frac{I_{DLL}}{I_0}e^{-\frac{V_y-V_{in}}{nV_T}}\right)=e^{\frac{-V_y}{nV_T}}, \quad (A.3)$$

which leads to

$$V_y=\frac{V_{in}}{2}+\frac{nV_T}{2}\log\left(1+\frac{I_{DLL}}{I_0}e^{-\frac{V_y-V_{in}}{nV_T}}\right). \quad (A.4)$$

Defining the DLS hysteresis threshold $V_{DLS,L}$ as the input voltage at which the source-gate voltage of MPU is zero as in [5], (A.4) leads to

$$V_{DSL,L}=nV_T\log\left(1+\frac{I_{DLL}}{I_0}\right). \quad (A.5)$$

which is about $3V_T \simeq 75$mV at room temperature, which agrees well with the simulated value of 70mV. Being I_{DLL} and I_0 weakly dependent on V_{DD}, $V_{DSL,L}$ is also nearly supply independent, as was observed in Fig. 4.

APPENDIX B. EVALUATION OF $V_{AB,H}$

The voltage $V_{AB,H}$ associated with the high output level of the G3a gate loaded by the active load G4a can be evaluated with the aid of the circuit in Fig. 6, when the input voltage is low and the leakage through capacitor C in Fig. 2 is neglected. Due to the short-circuited input/output connection of G4a, MN4a (MP4a) operates in the sub-threshold region with $v_{GS,MN4a}<0$ ($v_{SG,MP4a}<0$), and sets the current flowing through the diode-connected transistor MPU4a (MPD4a).

Under the same assumptions in Appendix A, G4a-b act as an active load delivering a current i_L that depends on v_{OUT} as in

$$i_L=I_P\left(1-e^{-\frac{v_{OUT}}{V_T}}\right)-I_N\left(1-e^{-\frac{V_{DD}-v_{OUT}}{V_T}}\right) \quad (B.1)$$

where $I_P=I_0e^{\frac{v_{SG,MP4a}}{nV_T}}$, $I_N=I_0e^{\frac{v_{GS,MN4a}}{nV_T}}$. Let us also assume that v_{OUT} is not very close to either ground or V_{DD} due to the presence of the active load, differing from them by at least three thermal voltages as in (B.2)

$$3V_T<v_{OUT}<V_{DD}-3V_T. \quad (B.2)$$

Under this assumption, the exponential terms in (B.1) are negligible compared to one, thus i_L is approximately equal to I_P-I_N. Hence, i_L depends only on the size of MN4a and MP4a, and is independent of V_{DD}.

Applying KVL to the output of the circuit in Fig. 6, $V_{AB,H}$ is equal to $V_{GS,MN3a}+V_{SG,MPU3a}$. In turn, $V_{GS,MN3a}$ and $V_{SG,MPU3a}$ are obtained by inverting (A.1) for MN3a and MPU3a transistors, which results to

$$V_{GS,MN3a}=nV_T\log\frac{i_L}{I_0}, \quad (B.3)$$

$$V_{SG,PU3a}=nV_T\log\frac{i_L}{I_P\left[1-\left(\frac{i_L}{I_0}\right)^n\right]} \quad (B.4)$$

which are both independent of the supply voltage at the first order. Indeed, V_T, i_L and I_0 are all supply-independent at first order in (B.3) and (B .4). As a consequence, $V_{AB,H}$ results to

$$V_{AB,H}=nV_T\left(log\left(\frac{i_L}{I_0}\right)^2\frac{1}{1-\left(\frac{i_L}{I_0}\right)^n}\right), \quad (B.5)$$

which numerically results to approximately 275mV at 0.4V, and is supply-independent at first order according to Fig. 7. From Fig. 8, $V_{AB,H}$ is actually slightly above 200mV (i.e., 25% less than (B.5)), since the capacitor leakage is not completely negligible compared to the very small super-cutoff current of MN4a, MPU4a, MPD4a, MP4a in Fig. 6. However, this does not affect the above conclusions at first order, being the capacitor leakage set by the voltage across it, and not V_{DD}.

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